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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,103	CHEN ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 11/02/2006 forms the basis for this office action. In said Amendment Applicant substantially amended all previously outstanding claims 1-13 and 15-22 and added new claim 24. Applicant also amended the specification. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claims 19-22*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. In particular, the limitation of "bitline diffusions" and "source diffusions" "spaced *alternately* in the active area with no other diffusions between them" as recited in claim 19, lines 2-3, is not supported by the original specification: no alternate spacing between source diffusions and bitline diffusions can be found in said original specification.

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claims 4, 18 and 22*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claimed inter-gate capacitance "large enough for voltage coupling between the gates during program and erase operations" introduces an indefinite inter-gate capacitance because there are three gates with three capacitances, namely: select gate – control gate, select gate – floating gate and control gate – floating capacitances, while the claimed program and erase operations have not been defined in quantitative electromagnetic terms and hence the conditions under which said voltage coupling exists is indefinite.
3. The term "relatively" in ***claim 3*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
4. The term "relatively low" in ***claim 9*** is a relative term, which renders the claim indefinite. The term "relatively low voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite

degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

5. The term "relatively high" in ***claim 9*** is a relative term, which renders the claim indefinite. The term "relatively high positive voltage" (lines 2-3, 4, 5, 6-7 and 8) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
6. The term "relatively high" in ***claim 10*** is a relative term, which renders the claim indefinite. The term "relatively high negative voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
7. The term "relatively low" in ***claim 10*** is a relative term, which renders the claim indefinite. The term "relatively low negative voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
8. The term "relatively high" in ***claim 11*** is a relative term, which renders the claim indefinite. The term "relatively high negative voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

9. The term "relatively low" in ***claim 11*** is a relative term, which renders the claim indefinite. The term "relatively low negative voltage" (lines 2-3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

10. The term "relatively" in ***claim 17*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

11. The term "relatively" in ***claim 21*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

12. The term "high-voltage" in ***claim 22*** is a relative term, which renders the claim indefinite. The term "high-voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1-13 and 15-18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (6,911,690 B2) (as previously made of record by examiner, see PTO-892) in view of Sakui et al (6,411,548 B1) and Chapman et al (6,118,161).

Hsu et al teach a NAND flash memory cell array (Figures 1A, 1B, title, abstract and column 4, line 55 – column 6, line 24), comprising:

A substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source region 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source region, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source region (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) positioned above a floating gate 118 (column 5, line 36). Furthermore, a bitline diffusion, i.e., diffusion region for a

bitline, inherently is contacted with a bitline: both bitline and bitline contact must therefore exist.

Hsu et al do not necessarily teach the last select gate in the row at least partially overlaps said source region. *However, it would have been obvious to include said limitation in view of Sakui et al,* who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region overlap (Figure 49; see also column 27, lines 43-49) (otherwise no overlap capacitance could exist). *Motivation* to include said teaching of overlap, between any select gate and source region derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by Chapman et al (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 2: clearly stacked gates and select gates are aligned to each other. The term "self-aligned" refers to the process of self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 3: the memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates

and control gates. Hsu et al do not necessarily teach said first and second dielectric to be thick in comparison with said (necessarily thin) tunnel oxide. However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling. Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 4: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates, whatever applicant intended to define as "gates" (Select gates? Floating gates? Control gates?; see above for rejection of this claim under 35 USC 112, second paragraph).

On claim 5: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted without giving weight to the limitation "high". Inherently, erase paths based on Fowler-Nordheim tunneling as exploited by Hsu et al extend from the floating gates, through the tunnel oxide to the channel regions by virtue of the very

existence of a current path for electrons between floating gate to the channel regions through Fowler-Nordheim tunneling (col. 8, l. 61-67), and voltage is coupled to the floating gates both from the control gates and from the select gates (keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin).

On claim 6: Program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates (because regions are conductive through the action of said gates, thereby allowing programming paths to exist); and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region (col. 3, l. 50-56): keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin. It is noted that the newly added limitations "below the floating gates" and "in the substrate" are met in any channel with lateral floating gates: the channel is located in the uppermost portion of the substrate abutting the interface between substrate and gate insulating layer. Therefore, said newly added limitations do nothing to further limit the cell array.

On claim 7: Program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates (because channel regions are highly conductive through the action of the gates and hence substantially conductive, thereby allowing programming paths to exist), while the remainder of the limitation defined by claim 7 constitutes functional language: In reference to the claim language

referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 8: The select gates in unselected cells *can be* biased at a relatively high voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source diffusion. Whether or not they are has no patentable weight: In reference to the claim language referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 9: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low positive voltage" and "relative high positive voltage" are terms merely indicating that the former voltage is lower than the latter voltage. The bit line for a row containing a selected cell to be programmed *can be*

held at 0 volts because said bit line is conductive; a relatively low positive voltage *can be* applied to a cell select gate for the selected cell as the select gates are independent; a relatively high positive voltage *can be* applied to the source diffusion at the second end of the row in which the selected cell is located because any source region is inherently conductive; a relatively high positive voltage *can be* applied to the control gate in the selected cell; a relatively high positive voltage *can be* applied to the select gates for unselected cells, and a relatively high positive voltage *can be* applied to the control gates in the unselected cells. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 10: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low negative voltage" and "relative high negative voltage" are terms merely indicating that the former voltage is lower in magnitude than the latter voltage. An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusions, the source diffusion and the P-well at 0 volts. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of

functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 11: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low negative voltage" and "relative high negative voltage" are terms merely indicating that the former voltage is lower in magnitude than the latter voltage. An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the active area at a positive voltage and the bit line and source diffusions floating. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 12: A read path *can be* formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells (cell selection being possible in the structure defined by Figures 3 and 4a,b), with the common source at 0 volts, the bit line diffusion at 1-3 volts, and the control gate at relatively high positive

voltage, and the control gate of the selected cell *can be* biased at 0-1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 13: As discussed under claim 11, an erase path *can be* formed by biasing of control gates and select gates; since this biasing can be done for each individual member in the cell array an erase path can erase the whole cell array simultaneously; and since cells can be selected individually a program path which is single cell selectable *can be* created through appropriate biasing. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 15: Hsu et al teach a NAND flash memory cell array (Figures 1A, 1B, title, abstract and column 4, line 55 – column 6, line 24), comprising:

a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source diffusion 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source diffusion (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) positioned above a floating gate 118 (column 5, line 36). Furthermore, a bitline diffusion, i.e., diffusion region for a bitline, inherently is contacted with a bitline: both bitline and bitline contact, if only in the form of a contact interface, must therefore exist.

Hsu et al do not necessarily teach the last select gate in the row being directly above said source region. *However, it would have been obvious to include said limitation in view of Sakui et al,* who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region showing said select gate directly above said source diffusion (i.e., a vertical line may be drawn intersecting both source diffusion and select gate (Figure 49; see also column 27, lines 43-49) (otherwise no overlap capacitance could exist). *Motivation* to include said teaching derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by Chapman et al (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 16: clearly stacked gates 118/122 and select gates 106 are aligned to each other (see Figures 1A and 1B). The term "self-aligned" refers to the process of "self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 17: the memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates and control gates. Hsu et al do not necessarily teach said first and second dielectric to be thick in comparison with said (necessarily thin) tunnel oxide. However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling. Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 18: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates, whatever applicant intended to define as "gates" (Select gates? Floating gates? Control gates? see above for rejection of this claim under 35 USC 112, second paragraph).

On Claim 24: Hsu et al teach a NAND flash memory cell array, comprising: a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source diffusion 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source diffusion (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) and a floating gate 118 (column 5, line 36) with aligned sides adjacent to the select gates (Figure 1B), erase paths between the floating gates and channel regions in the active area beneath the stacked gates (col. 8, lines 61-67). The limitation "self-aligned" rather than merely "aligned" only further introduces a limitation on the method of making said memory cell array and fails to further limit the invention claimed here as a final structure only. Furthermore, voltage coupling from the control gates to the floating gates inherently exists because the control gates control by definition the voltage of the floating gates so as to control the number of charge carriers in said floating gates while voltage coupling between select gates and floating gates inherently exists because the select gates

determine whether or not a channel exists along which charge carriers can approach said floating gates.

Response to Arguments

Applicant's arguments filed 11/02/05 have been fully considered but they are not persuasive. Applicants substantially amended all previously outstanding claims. The objection to the Drawings has been withdrawn in light of Applicant's Remarks. However, The claimed invention is obvious over Hsu et al previously made of record (see PTO-892), as shown in the rejections overleaf. With regard to the traverse of claim 2 on the basis of the limitation "self-aligned" it is pointed out that self-aligned means aligned other than an implied limitation on the method of making irrelevant for the claimed invention, for which only the final structure matters. With regard to Remarks on capacitance between "the" gates, "the gates" in the context of the claimed invention is indefinite because there are three independent capacitances between three different pairs of gates, while capacitance does not need specific teaching since it is inherently there: a control gate, otherwise materially isolated from the floating gate, otherwise would have no function at all, the latter being the influence on charge carriers at a quantum-mechanical scale distance from the floating gate, while the very existence of conducting areas separated by a dielectric (spacer 114). Although Noda has been withdrawn, there was no strict necessity to do so for most limitations, NAND flash memory not being in the bulk of the claim language. However, in the examiner's opinion, after amendment Hsu et al is the best reference, whence the above rejections. Finally, it is noted that, although no art has

been found for claims 19-22, claims 19-22 constitute new matter (see rejections under 35 USC 112, first paragraph) because the limitation of "bitline diffusions" and "source diffusions" "spaced *alternately* in the active area with no other diffusions between them" as recited in claim 19, lines 2-3, is not supported by the original specification: no alternate spacing between source diffusions and bitline diffusions can be found in said original specification.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
January 5, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER